REMARKS

This Amendment is submitted in response to the Office Action dated March 23, 2005, having a shortened statutory period set to expire June 23, 2005.

In paragraph 2 of the present Office Action, Figures 1A and 2 are objected to for failing to include the legend "Prior Art". In response, Applicant has proposed amendments to Figures 1A and 2 to include the legend "Prior Art." The proposed amendments do not include any new matter.

In paragraph 5 of the present Office Action, the Examiner states that the incorporation by reference of the O'Brien article at page 15 of the specification is improper. Applicant does not believe that the incorporation is improper because MPEP 608.01(p) clearly permits the incorporation of non-essential subject matter from non-patent publications:

> Nonessential subject matter may be incorporated by reference to (1) patents or applications published by the United States or foreign countries or regional patent offices, (2) prior filed, commonly owned U.S. applications, or (3) non-patent publications however, aperients and/or other forms of browser executable code cannot be incorporated by reference. See MPEP § 608.01. Nonessential subject matter is subject matter referred to for purposes of indicating the background of the invention or illustrating the state of the art. (emphasis supplied)

In the present case, the O'Brien reference is incorporated to illustrate the state of the art, and in particular, to provide a detailed example of how to compute the components of a pi-model of equivalent effective capacitance. This material is non-essential in that it details one of many possible conventional modeling schemes (e.g., pi-model, tee-model, etc.) that can be employed and is not necessary to (1) describe the claimed invention, (2) provide an enabling disclosure of the claimed invention, or (3) describe the best mode.

Next, in paragraph 7.1, Claims 1-5, 8-12 and 15-19 are rejected under 35 U.S.C. § 102(e) as unpatentable over U.S. Patent No. 6,347,393 to *Alpert*. In addition, in paragraph 8.1, Claims 6-7, 13-14 and 20-21 are rejected under 35 U.S.C. § 103 as unpatentable over *Alpert* in view of Qian et al., "Modeling the 'Effective Capacitance' for the RC Interconnect of CMOS Gates"

(*Qian*). Those rejections are respectfully traversed, and favorable consideration of the claims is requested.

Applicant respectfully submits that exemplary Claim 1 is not rendered unpatentable by *Alpert* because that reference does not teach or suggest each of the features recited therein. For example, *Alpert* does not teach or suggest "utilizing said equivalent effective capacitance value to calculate said interconnect delay at said node," as recited in exemplary Claim 1. With respect to this feature, paragraph 7.1.1 of the present Office Action cites col. 10, lines 1-20 of *Alpert*, which discloses a three step approach for using effective capacitance to calculate gate (not interconnect) delay at a node (see also, e.g., col. 9, lines 65-67). The distinction between the gate delay relied upon by the Examiner and the interconnect (wire) delay recited in exemplary Claim 1 is explained by *Alpert* at col. 6, line 56 through col. 7, line 5, and particularly in Equation 1, which discloses that the total path delay between a source and a sink is computed by summing the gate delay and wire delay at each node in the path.

It should further be noted that *Alpert* does disclose a technique for calculating interconnect (wire) delay at a node at col. 11, line 56 through col. 12, line 67. In this technique, the circuit moments of the nodes in the interconnect path are first computed according to Equations 6-8. Next, the poles and residues of a second order approximation of the sum of the moments are determined in accordance with Equations 9-11. Finally, the interconnect (wire path) delay is computed via a Newton-Raphson iteration (col. 12, lines 64-67). Importantly, the effective capacitance at a node (C_{eff}) is not a term in any of the equations utilized by *Alpert* to compute the interconnect delay.

Because *Alpert* does not teach or suggest the use of equivalent capacitance to calculate an interconnect delay at a node and instead teaches an alternative approach that does not employ a calculation of effective capacitance, Applicant respectfully submits that the rejections of exemplary Claim 1, similar Claims 8 and 15 and their respective dependent claims are overcome. Applicant further believes that newly entered Claims 22-23, which similarly recite the use of the effective capacitance to determine interconnect delay, are patentable over *Alpert* and the other prior art of record for the reasons set forth above.

Having now responded to each objection and rejection set forth in the present Office Action, Applicant believes all pending claims are now in condition for allowance and respectfully requests such allowance.

Please charge IBM Corporation Deposit Account No. **09-0447** in the amount of $300.00 for 1 additional independent claim in excess of 3 and 2 additional claims in excess of 20. No additional fee is believed to be required. If, however, any additional fees are required, please charge those fees to IBM Corporation Deposit Account No. **09-0447**.

Respectfully submitted,

Brian F. Russell
Registration No. 40,796
DILLON & YUDELL LLP
8911 N. Capital of Texas Hwy., Ste. 2110
Austin, Texas 78759
(512) 343-6116

ATTORNEY FOR APPLICANT

DRAWINGS

Please amend Figures 1A and 2 as indicated on the attached Replacement Sheets.